REMARKS

Status of Claims

Claims 6-10 are pending in this application.

Claim Rejections – 35 USC §101

Claims 6-10 were rejected under 35 USC § 101 as being non-statutory subject matters. Claims 6-10 have been amended to overcome the rejections.

Claim Rejections – 35 USC §103

Claims 6-10 were rejected under 35 USC § 103 as being unpatentable over Berenbaum et al in view of Zalamea et al.

The Applicant, in view of the amendments, respectfully traverses the rejections with the following arguments.

[Argument 1]: The cited prior art, Berenbaum et al, teaches a multithreaded processor processes each thread with a designated register file. All threads share the same functional unit. The crossbar switch as taught by Berenbaum et al accesses the operands from the designated register file of each thread for process. However, the current invention disclosed one register file for a function unit being partitioned into global and local register files. The architecture of the current invention is different from what was taught by the cited prior art.

[Argument 2]: The cited prior art, Zalamea et al, teaches partitioning the shared registered file into clustered registered file. Zalamea et al teaches storing data at the shared register file for operation access. However, the current invention does not transfer the data for operation access. The cluster communication disclosed by the current invention is maintaining the data at the original register file without transfer the data before the operation access. The

operation data access of the current invention is a direct access in accordance with the mapping relation.

[Argument 3]: The current invention teaches "the clustered functional units exchanging data by permutations of the sub-register files ....., without transferring the data". The cited prior art failed to teach the claimed limitation. Examiner is respectfully requested to provide a *prima facie* evidence for such a rejection.

[Argument 4]: The current invention teaches "the data exchange is a direct data access in accordance with the mapping relationship". The cited prior art failed to teach the claimed limitation. Examiner is respectfully requested to provide a *prima facie* evidence for such a rejection.

[Argument 5]: The current invention claims "the clustered functional units exchange data by permutation of the sub-register files of the at least one global register file through setting crossbar switches". The cited prior art, Berenbaum et al, failed to teach the claimed limitation. Examiner is respectfully requested to provide a prima facie evidence for such a rejection.

[Argument 6]: The current invention claims "the permutation maps the sub-register files of the at least one global register file to the clustered functional units." The cited prior art, Berenbaum et al, failed to teach the claimed limitation. Examiner is respectfully requested to provide a prima facie evidence for such a rejection.

In view of the amendments and remarks, Applicant submits that all of the pending claims are in condition for allowance and requests early and favorable action on the merits. The Examiner is invited to telephone the undersigned, Applicant's Attorney of Record, to facilitate advancement of the present application.

Respectfully submitted,

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Date

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